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10/675,027	09/30/2003	Dennis Kim	RAMB-01016US0	5412

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EXAMINER	
PANWALKAR, VINEETA S	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/675,027	KIM ET AL.	
	Examiner	Art Unit	
	Vineeta S. Panwalkar	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-8 and 10-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3,5-8 and 10-24* is/are allowed.

6)☒ Claim(s) *25-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 4/12/07 have been fully considered but they are not persuasive.

1a. Regarding claim 25, applicant claims that Chiu (US 6642747 B1, hereinafter, Chiu) discloses claimed phase detector, but fails to disclose claimed clock circuit. However, applicant is referred to column 1, lines 1- 45 and Fig.4. The phase locked loop (PLL) circuit shown in Fig. 4 is interpreted as the claimed clock circuit because the voltage controlled oscillator (VCO) 450 generates a clock signal in response to a control signal corresponding to the phase adjustments needed. As for the claimed averaging circuit, applicant is referred to column 8, line 61 – column 9, line 27. Over a given time interval, the average value of the UP1 and DOWN1 signals will correspond to the phase difference between the VCO_CLK signal and the REF_CLK signal. Thus, the clock circuit (PLL) comprises the averaging circuit. Thus, Chiu does indeed disclose claimed clock circuit.

1b. Regarding claims 29-33, the motivation to use the averaging circuit suggested by Chiu in the PLL circuit suggested by Behrens (US 5572558, hereinafter Behrens) is further clarified. The averaging circuit provided by Chiu smoothens out the control signal used to adjust phase and frequency of the VCO (Column 1, lines 20-35). Thus, Chiu's averaging circuit better controls the adjustment of the phase

and frequency of the VCO of the PLL. Hence, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the averaging circuit disclosed by Chiu because the UP and DOWN signals in the circuit allow the PLL to adjust the phase and frequency of the VCO in the manner disclosed by Chiu (i.e. with more control over the adjustment).

1c. Thus, the rejection mailed 10/13/06 is maintained and follows hereinafter. (The rejection of claim 25 has been changed to address the limitations of the amended claim 25).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 25 is rejected under 35 U.S.C. 102(e) as being anticipated by Chiu (US 6642747 B1), hereinafter, Chiu.

2a. Regarding claim 25, Chiu discloses a phase locked loop (PLL) system (claimed circuit) comprising:

- a sampler configured to receive a data signal in response to the clock signal (Fig. 4, the phase-locked loop (PLL) can be used as a clock generator in an analog/digital conversion system (claimed sampler). Column 1, lines 12-17);
- a phase detector to output a plurality of up signals and a plurality of down signals in response to the data signal (Column 7, lines 43-63 and Fig. 4, phase detector 410);
- a clock circuit configured to generate the clock signal in response a phase adjust signal (the PLL is interpreted as the claimed clock circuit because the voltage controlled oscillator (VCO) generates a clock signal in response to a control signal corresponding to the phase adjustments needed (column 1, lines 10- 45)); and
- wherein the clock circuit comprises, an averaging circuit capable to output the phase adjust signal in response to an average up signal, obtained from a plurality of up signals in a predetermined period of time, and an average down signal, obtained from a plurality of down signals, in the predetermined period of time (Fig. 4. Phase detector 410 is arranged to produce a first up and down signal (UP1, DOWN1) in response to comparing the phases between a reference clock signal (REF_CLK) and a VCO output clock signal (VCO_CLK). Over a given time interval, the average value of the UP1 and DOWN1 signals will correspond to the phase difference between the

VCO_CLK signal and the REF_CLK signal. The phase-detector is thus employed to adjust the phase relationship between the VCO clock signal and the reference clock signal. Column 7, lines 52-60; column 8, line 61 – column 9, line 27).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chui in view of Shastri (US 2002/0105386 A1).

3a. Regarding claim 26, Chiu discloses all the limitations claimed (see 2a above). However, Chui fails to explicitly disclose claimed counter.

In the same field endeavor however, Shastri discloses a clock recovery circuit, wherein is disclosed a counter capable of outputting phase adjust signal. (Figs 12,13 and 14. Counter 41 takes in UP4 and DOWN4 signals. The output of the counter 41 is fed to a comparator 43 (paragraphs [0067]- [[0068]) and then is further used to output a phase adjust signal (paragraph [0094]). Thus, counter 41 is required to generate the phase adjustment and is hence interpreted as claimed mixer counter).

Thus, it would have been obvious to a person of ordinary skill in the art to use the circuit suggested by Shastri because it prevents glitches in the generated clock. (Paragraph [0012]).

3c. Regarding claim 27, Chiu discloses all the limitations claimed (see 2a above). However, Chui fails to explicitly disclose claimed counter.

In the same field endeavor however, Shastri discloses a clock recovery circuit, wherein:

- the averaging circuit includes a comparator circuit, capable of adjusting the phase adjust signal in response to a comparison of the average up value and

the average down value. (Figs 12,13 and 14. Counter 40 keeps a running average of the up and down indications of the phase detector and outputs UP4 and DOWN4. Slow filter 47 keeps track of the average of the UP4/DOWN4 signals thereby maintaining a running average of the total UP/DOWN indication count. A rollover and resulting PHUP or PHDOWN signifies that there is a strong indication that the RCK has drifted permanently away from the phase of the input data DIN, i.e. indicating phase adjust. (See paragraph [0091],[0092]). Thus, counter 41 takes in UP4 and DOWN4 signals and the output of the counter 41 is fed to a comparator 43 (paragraphs [0067]- [[0068]) and then is further used to output a phase adjust signal (paragraph [0094])).

Thus, it would have been obvious to a person of ordinary skill in the art to use the circuit suggested by Shastri because it prevents glitches in the generated clock. (Paragraph [0012]).

4. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chui in view of applicants' own admitted prior art, hereinafter, AOAPA.

4a. Regarding claim 28, Chiu discloses all the limitations claimed (see 2a above). However, Chui fails to explicitly disclose the exact applications of the system in detail.

In the same field endeavor however, AOAPA discloses that a clock-data recovery circuit, such as the one claimed, is included in a receive circuit coupled to a transmit circuit capable of transmitting the data signal.(Page 1, lines 18-26 of specification).

Thus, it would have been obvious to a person of ordinary skill in the art to use Chui's circuit in a transmit/receiver circuit as disclosed by AOAPA in order to synchronize a sample clock with incoming data.

4. Claims 29-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beherns (US 5572558, previously cited) in view of Chui.

5a. Regarding claim 29, Beherns discloses a timing recovery phase locked loop (PLL) for synchronizing the sampling of a received signal wherein is disclosed an apparatus comprising:

- a transmit circuit capable of transmitting a data signal having a variable rate (Broadly speaking, Fig.1 shows a system wherein data is encoded using units 4,6,10 and 14 (claimed transmit circuit) to form symbols 16 (claimed data signal) that are transmitted via magnetic recording channel 18. The data rate of the signal is varying. (Column 5, lines 1-23 explain how the data rate varies from track to track of the disk which stores the data)).
- A receive circuit capable of generating a clock signal in response to the data signal.(Fig.3 also shows the circuit that receives data encoded by a system

such as the transmitter of Fig.1 and performs timing recovery and is hence interpreted as the claimed receive circuit).

- wherein the receive circuit includes:
- a sampler, capable of receiving, in response to the clock signal, in response to the clock signal (The analog to digital converter (A/D) 24 is the claimed sampler. VFO F50 provides a clock signal to the sampling device 24. It receives the analog read signal 11.).
- a clock circuit, coupled to the sampler, (Fig. 3, unit 28 is interpreted as the claimed clock circuit) capable of generating a clock signal in response to an adjustable phase step-size (VFO F50 provides a clock signal to the sampling device 24 based on the error signals provided by the phase and frequency error detectors F54 and F52. The phase error signal F123 output by phase error detector F54 inherently indicates the amount (claimed step-size) of adjustment required to be made to the phase of the clock signal and is hence interpreted as the claimed adjustable phase step-size).

(See Fig.3 and column 8, lines 15-30).

Thus, Beherns discloses all the limitations claimed, but fails to explicitly disclose whether the PLL consists of an averaging circuit.

In the same field of endeavor, however, Chui discloses a PLL system (claimed clock circuit) comprising:

- an averaging circuit capable to output the phase adjust signal in response to an average up signal, obtained from a plurality of up signals in a

predetermined period of time, and an average down signal, obtained from a plurality of down signals, in the predetermined period of time (Fig. 4. Phase detector 410 is arranged to produce a first up and down signal (UP1, DOWN1) in response to comparing the phases between a reference clock signal (REF_CLK) and a VCO output clock signal (VCO_CLK). Over a given time interval, the average value of the UP1 and DOWN1 signals will correspond to the phase difference between the VCO_CLK signal and the REF_CLK signal. The phase-detector is thus employed to adjust the phase relationship between the VCO clock signal and the reference clock signal. Column 7, lines 52-60; column 8, line 61 – column 9, line 27).

Thus, it would have been obvious to a person of ordinary skill in the art to use the averaging circuit disclosed by Chui because the UP and DOWN signals in the circuit allow the PLL to adjust phase and frequency of the VCO.

5b. Regarding claim 30, Beherns discloses a timing recovery phase locked loop (PLL) for synchronizing the sampling of a received signal wherein is disclosed a method for tracking a variable data rate signal (The data rate of the signal is varying. (Column 5, lines 1-23 explain how the data rate varies from track to track of the disk which stores the data)) comprising the steps of:

- receiving the signal .(Fig.3 shows the circuit that receives data 11 and performs timing recovery).;

- selecting an update rate(Fig. 3, unit 28 is clock circuit comprising VFO F50. VFO F50 provides a clock signal to the sampling device 24 based on the error signals provided by the phase and frequency error detectors F54 and F52. Thus, the timing recovery loop synchronizes values sampled by the sampling device 24 at a rate determined by the VFO F50. This is interpreted as the claimed selecting of an update rate); and
- selecting an adjustable step-size for an adjust signal responsive to the signal (Fig. 3, unit 28 is clock circuit comprising VFO F50. VF50 provides a clock signal to the sampling device 24 based on the error signals provided by the phase and frequency error detectors F54 and F52. The phase error signal F123 output by phase error detector F54 inherently indicates the amount (claimed step-size) of adjustment required to be made to the phase and frequency of the clock signal and this operation is hence interpreted as the claimed selecting of adjustable step-size for an adjust signal).

(See Fig.3 and column 8, lines 15-30).

Thus, Beherns discloses all the limitations claimed, but fails to explicitly disclose whether the PLL consists of an averaging method.

In the same field of endeavor, however, Chui discloses a PLL system wherein is disclosed a method including:

- averaging a plurality of up signals to obtain an average up value; averaging a plurality of down signals to obtain an average down value; outputting the adjust signal in response to the average up value and average down value.

(Fig. 4. Phase detector 410 is arranged to produce a first up and down signal (UP1, DOWN1) in response to comparing the phases between a reference clock signal (REF_CLK) and a VCO output clock signal (VCO_CLK). Over a given time interval, the average value of the UP1 and DOWN1 signals will correspond to the phase difference between the VCO_CLK signal and the REF_CLK signal. The phase-detector is thus employed to adjust the phase relationship between the VCO clock signal and the reference clock signal. Column 7, lines 52-60; column 8, line 61 – column 9, line 27; also, see column 5, line 7 – line 35).

Thus, it would have been obvious to a person of ordinary skill in the art to use the averaging circuit disclosed by Chui because the UP and DOWN signals in the circuit allow the PLL to adjust phase and frequency of the VCO.

5c. Regarding claim 31, Beherns further shows the method wherein the receiving step includes:

- sampling the signal in response to the adjust signal (The analog to digital converter (A/D) 24 performs the claimed sampling. It receives the analog read signal 11).

5d. Regarding claim 32, Beherns also shows the method wherein selecting an adjustable step-size includes:

- determining a first step-size based on the variable data bit- rate of the signal (Fig. 3, phase error detector F54, provides a phase error signal F123 indicating the amount (claimed first step-size) of adjustment required to be made to the phase of the clock signal. It takes into account the variable data bit-rate via signal 27. This is because signal 27 is the sampled and equalized version of the variable rate received signal);
- determining a second step-size (Fig. 3, frequency error detector F52 provides a frequency error signal F124 indicating the amount (claimed second step-size) of adjustment required to be made to the frequency of the clock signal);
- summing the first and second step-sizes to obtain the adjustable step-size (Fig. 3. PID loop filter F56 sums the two signals F123 and F124 to form signal 23, which adjusts the sampling clock. See Fig. 9B and column 9, line 21 – column 10, line 63).

(See Fig.3 and column 8, lines 15-30).

5e. Regarding claim 33, Beherns discloses a timing recovery phase locked loop (PLL) for synchronizing the sampling of a received signal wherein is disclosed a clock circuit (claimed device) comprising:

- a sampler capable of obtaining a signal having a variable data bit-rate in response to a clock signal (The analog to digital converter (A/D) 24 is the claimed sampler. VFO F50 provides a clock signal to the sampling device 24. It receives the analog read signal 11 with varying data rate (Column 5, lines

1-23 explain how the data rate varies from track to track of the disk which stores the data)); and

- means for adjusting the clock signal in response to the variable data bit-rate (Fig. 3, unit 28 is capable of generating a clock signal in response to an adjustable phase step-size. VFO F50 provides a clock signal to the sampling device 24 based on the error signals provided by the phase and frequency error detectors F54 and F52. The error detectors take into account the variable data rate via signal 27. This is because signal 27 is the sampled and equalized version of the variable rate received signal).

(See Fig.3 and column 8, lines 15-30).

Thus, Beherns discloses all the limitations claimed, but fails to explicitly disclose whether the PLL consists of an averaging circuit.

In the same field of endeavor, however, Chui discloses a PLL system (claimed device) comprising:

- means for adjusting the clock signal in response to a phase adjust signal, wherein the means for adjusting includes an averaging means for outputting the phase adjust signal in response to an average up signal, obtained from a plurality of up signals in a predetermined period of time, and an average down signal, obtained from a plurality of down signals, in the predetermined period of time (Fig. 4. Phase detector 410 is arranged to produce a first up and down signal (UP1, DOWN1) in response to comparing the phases between a reference clock signal (REF_CLK) and a VCO output clock signal

(VCO_CLK). Over a given time interval, the average value of the UP1 and DOWN1 signals will correspond to the phase difference between the VCO_CLK signal and the REF_CLK signal. The phase-detector is thus employed to adjust the phase relationship between the VCO clock signal and the reference clock signal. Column 7, lines 52-60; column 8, line 61 – column 9, line 27).

Thus, it would have been obvious to a person of ordinary skill in the art to use the averaging circuit disclosed by Chui because the UP and DOWN signals in the circuit allow the PLL to adjust phase and frequency of the VCO.

Allowable Subject Matter

6. Claims 1-3, 5-8, 10, 12-24 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

6a. Regarding claim 1, prior art of record fails to show a circuit comprising a clock generating circuit capable of generating a clock signal in response to and adjustable phase step-size and sampler with a data signal having a variable rate and including at least four stages wherein the clock circuit includes stall logic for capable of holding the third and fourth stage outputs in response to the first and second stage outputs, in combination with every other limitation of the claim. The claim is interpreted in light of the specification, especially Figs 1 and 5.

6b. Claims 2,3,5-8, 12 and 13 are allowed as being dependent on claim 1.

6c. Regarding claim 10, prior art of record fails to show the circuit comprising capable of generating a clock signal in response to and adjustable phase step-size and sampler with a data signal having a variable rate, wherein the clock circuit includes a counter for obtaining a first step-size and the indicator provides a second step-size, wherein the first step size and the second step size are summed to obtain the adjustable phase step-size, in combination with every other limitation of the claim. The claim is interpreted in light of the specification, especially Figs. 1 and 7.

6d. Claim 11 is allowed as being dependent on claim 10.

6 e. Regarding claim 14, prior art of record fails to show a circuit with a clock circuit comprising a first stage, coupled to the sampler, capable of outputting a first stage output signal in response to the data signal; a second stage, coupled to the first stage, capable a second stage output signal in response to the first of outputting stage output signal', a third stage, coupled to the second stage, capable outputting the phase adjust signal in response to the second stage output signal; and stall logic, coupled to the first, second and third stages, and capable of holding the phase adjust signal in response to the first and second stage output signals, in combination with every other limitation of the claim. The claim is interpreted in light of the specification, especially Figs 1 and 5.

6f. Claims 15-17 will be allowable as being dependent on claim 14.

6g. Regarding claim 18, prior art of record fails to show a circuit with a clock circuit comprising a first stage, coupled to the sampler, capable of outputting a first

stage output signal in response to the data signal; a second stage, coupled to the first stage, capable of outputting a second stage output signal in response to the first stage output signal; a third stage, coupled to the second stage, capable of outputting the phase adjust signal, having a first step-size, in response to the second stage output signal; stall logic, coupled to the first, second and third stages, capable of holding the phase adjust signal in response to the first and second stage output signals; an indicator, coupled to the third stage, capable of outputting a second step-size in response to the variable data bit- rate; and, a counter, coupled to the third stage and the indicator, capable of outputting the phase adjust signal having an adjustable step-size responsive to the first and second step-sizes, in combination with every other limitation of the claim. The claim is interpreted in light of the specification, especially Figs 1, 5 and 7.

6h. Claims 19-24 are allowed as being dependent on claim 18.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory

period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vineeta S. Panwalkar whose telephone number is 571-272-8561. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

VP

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER